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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,226	06/26/2003	Hideaki Watanabe	024016-00063	3751

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EXAMINER	
NGUYEN, HIEP	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 05/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,226	WATANABE, HIDEAKI	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3 and 5-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3 and 5-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The amendment filed on 02-28-05 has been carefully considered. However, the claims remained rejected under Kokubo. However, the rejections are changed because of the amendment of the claims.

Claim Objections

Claim 3 is objected to because of the following informalities: the recitation "wherein the counter is a counter for obtaining the count value at the end of every High level period and every Low level period" is not clear because it is not clear as to the high/low level period is the high/low level period of the reference clock signal or the high/low level period of the output clock signal. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 11 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required

Regarding claim 11, the recitation "a reference value" on line 8 is indefinite because it is not clear as to this "a reference value" is signal (SR) or signal (ST) in figure 8.

Claim 12 is indefinite because of the technical deficiency of claim 11.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3 and 5-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Kokubo et al. (US Pat. 5,928,208).

Regarding claim 1, figures 4 and 11 of Kokubo show a clock multiplication circuit for delivering an output clock signal at a frequency that is a multiple of the frequency of a reference clock signal as inputted, the clock multiplication circuit comprising:

a counter (5) for delivering a count value (Nv) by counting the number of effective transition edges of the output clock signal, existing during a predetermined counting period given on the basis of the reference clock signal (fref);

a subtracter (17) for delivering a difference value obtained by subtracting either the count value or a reference value from the other;

a control voltage generation circuit (18, 9, 4) for delivering an analog control voltage (Vr) corresponding to an integrated value of the difference value; and

a voltage control oscillator circuit (1) for delivering the output clock signal at a frequency corresponding to the analog control voltage (Vr). Figures 4 and 11 of Kokubo shows that the counter (5) delivers a count value (Nv) by counting the number of the effective transition edges of the output clock signal (fout) existing during counting period when the reference clock signal (fref) is either at high level or low level, the counter (5), the subtracter (17), control voltage generation circuit (18, 9, 4) and the voltage control oscillator circuit (1) having response characteristic such that when the control value (Nv) is changed from a preceding count value, the frequency of the output clock signal is changed after the end of the counting period and before the start of a succeeding counting period. Note that in figure 4, lines (B) and (C) shows that the count value (Nv) changes at the end of the counting period and before the start of a succeeding counting period (B is high) and at these moments, the count value changes (col. 4, lines 1-17) thus, the frequency of the output clock signal changes.

Regarding claim 3, figures 4 and 11 of Kokubo show a clock multiplication circuit comprising: a counter (5), a subtracter (17), a control voltage generation circuit (18, 9, 4) and a voltage control oscillator circuit (1). The counter (5) generates a count value (Nv) at the end of the high/low level period of the reference clock signal (fref).

Regarding claims 5-9, figures 4, 11 and 8 of Kokubo show a clock multiplication circuit for delivering an output clock signal that is a multiple of a reference clock signal

comprising: a counter (5), a subtracter (17), a control voltage generation circuit (18, 9, 4) generating the analog control voltage (Vr), a voltage control oscillator circuit (1). Counter (5) generates a count value (Nv) in synchronism with the output clock signal (fout). Subtractor (17) generates the difference value after the end of the counting period. The control voltage generation circuit generates the analog control voltage (Vr) after the end of the counting period and in synchronism with the output clock signal. The reference clock (fref) is the clock for the counter (5). The counter counts the frequency of the output clock (fout) that includes low and high level or in other word, including falling/rising edges. The multiplier (10, 18) comprises a shift register (18). The factor of the multiplier depends on a factor that is the bits of the subtractor (17) thus this factor is variable (col. 7, lines 4-11).

Regarding claim 10-12, the factor control means is element (10). The value of the factor varies by closing or opening switches (SW3) and (SW4) in figure 8. Controller (10) initializes the multiplier (18) with different digital values (col. 3 lines 60-64). The storage means is element (11). In claim 11, the subtractor (11) is capable of switching the reference value (N) (col. 7, lines 22-29). Memory device (6) stores the reference value (col. 3, lines 23-25).

Conclusion

THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen
05-04-05

TUAN T. LAM
PRIMARY EXAMINER